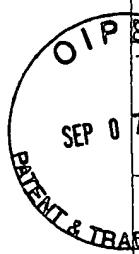


Form PTO-1449	Document Number (Case)	Assignment Number
INFORMATION DISCLOSURE CITATION IN AN APPLICATION		TSMC - 00 - 004 09/604, 067
(Use several sheets if necessary)		Applicant Ming - Dou Ker et al.
Mailing Date 06/26/00		Cross Ref. No. 1

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CASE	NUMBER	MUNO DATE X APPROPRIATE
DR	S 086365	2/4/92	Lien	361	58	5/8/90
JK	S 631793	5/20/97	Ker et al.	361	56	9/5/95
JL	48556208	8/8/89	Duvvury et al.	307	448	11/18/87
JL	52373958	8/17/93	Lee	257	358	5/28/91
DEPARTMENT	5255146	10/19/93	Miller	361	56	8/29/91
JL	5287241	2/15/94	Puar	361	56	2/4/92
JL	53113915	10/94	Dungan et al.	361	56	5/4/93
JL	54401628	8/8/95	Worley et al.	257	355	7/26/94
JR	56107913	11/97	Voldman	361	56	9/6/95
JR	56252804	12/97	Voldman	323	284	10/30/95



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OTHER DOCUMENTS (Including Author, Title, Date, Portion or Pages, Etc.)

IR Stephen G. Beebe, "Methodology for Layout Design and Optimization of ESD Protection Transistors," 1996 EOS/ESD Symp. Proc., pp. 265-275

IR Polgreen et al., "Improving the ESD Failure Threshold of Silicide n-MOS Output Transistors by Ensuring Uniform Current Flow," IEEE Trans. Electron Devices, Vol. 39, pp. 379-388, 1992.

BY JAMES R.

Izabel Sodré

DATE CONSIDERED

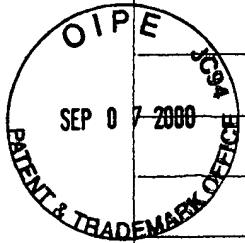
1 / 8 / 63

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Form PTO-1449	Document Number (Case)	Issue Date
INFORMATION DISCLOSURE CITATION IN AN APPLICATION		09/604,067
(Use several sheets if necessary)	Applicant	Ming - Dou Ker et al.
	Filing Date	06/26/00
	Drawn At U.S.	

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EXAMINER NAME	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	REG'D DATE X APPROPRIATE



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JR Duvvury et al., "Dynamic Gate Coupling of NMOS for Efficient Output ESD Protection", Proc. of IRPS, 1992, pp. 141-150.

JR Duvvury et al., "Achieving Uniform nMOS Device Power Distribution for Sub-micron ESD Reliability", Tech. Dig. IEDM, 1992, pp. 131-134.

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DATE CONSIDERED

1/8/03

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Form PTO-1449	Date Received (Year)	Received from
INFORMATION DISCLOSURE CITATION IN AN APPLICATION		
(Use several sheets if necessary)	Applicant	Ming-Dou Ker et al.
	Filing Date	06/26/00

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JR Ramaswamy et al., "EOS/ESD Reliability of Deep Sub-Micron NMOS Protection Devices", Proc. of IRPS, 1995, pp. 284-291.

JR Ker et al., "Capacitor-Coupled ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS ASIC", IEEE Trans. on VLSI Systems, Vol. 4, pp. 307-321, Sept. 1996.

CHAMBER

EXAMINER Gale Boleyn

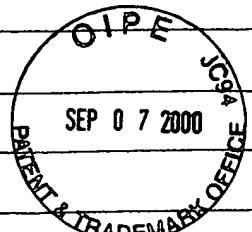
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Form PTO-1449	Document Number (Create)	Registration Number
INFORMATION DISCLOSURE CITATION IN AN APPLICATION		TSMC-00-004 09/604,067
(Use several sheets if necessary)		Applicant Ming - Dou Ker et al.
Filing Date 06/26/00		Group Art Unit

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JR
Ming-Dou Ker, "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuits for Submicron CMOS VLSI", IEEE Trans. on Electron Devices, Vol. 46, No. 1, pp. 173-183, Jan. 1999.

JF Merrill et al., "ESD Design Methodology, EOS/ESD Symp. Proc., 1994, EOS-16, pp. 141-149.

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Form PTO-1449	Document Number (Case)	Lightbeam Number
INFORMATION DISCLOSURE CITATION IN AN APPLICATION	TSMC-00-004	09/604,067
(Use several sheets if necessary)	Applicant	Ming-Dan Ker et al.
	Filing Date	06/26/00
	Drawn At UVI	

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Worley et al., "Sub-Micron Chip ESD Protection Schemes which Avoid Avalanche Junctions", EOS/ESD Symp. Proc., 1995, EOS-17, pp. 13-20.

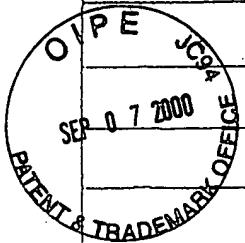
Examiner

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Form PTO-1449	Document Number (Optional)	Registration Number
INFORMATION DISCLOSURE CITATION IN AN APPLICATION		TSMC - D0 - 004 09/604,067
(Use several sheets if necessary)		Applicant Ming - Don Ker et al.
		Filing Date 06/26/00 Group Art Unit

U. S. PATENT DOCUMENTS



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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (*Including Author, Title, Date, Portion or Pages, Etc.*)

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Haldeman et al., "Scaling, Optimization and Design
Considerations of Electrostatic Discharge Protection
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Amerasekera et al., "The Impact of Technology Scaling on ESD Robustness and Protection Circuit Design", EOS/ESD Symp. Proc., pp. 237-245, 1994.

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~~DATE CONSIDERED~~

Saleh H. Al-Hajj

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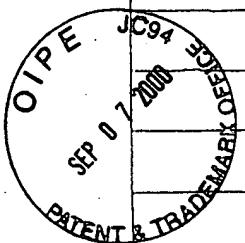
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Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)				Document Number (Original) TSMC -00-004	Date Entered 09/04/067	
				Applicant Ming-Dou Ker et al.		
				Filing Date 06/26/00	Drawn At U.S.	
U. S. PATENT DOCUMENTS						
EXAMINER NAME	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	
FOREIGN PATENT DOCUMENTS						
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES NO
OTHER DOCUMENTS (Including Author, Title, Date, Page No., Etc.)						
<i>JF</i>	Daniel et al., "Process and Design Optimization for Advanced CMOS I/O ESD Protection Devices", EOS/ESD Symp. Proc. pp. 206-213, 1990.					
<i>JF</i>	Chen et al., "Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes", Proc. of EOS/ESD Symp., pp. 230-239, 1997.					
EXAMINER <i>Isabel Borling</i>	DATE CONSIDERED 1/8/03					

EXAMINER: Initial if citation considered, wbcber or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Form PTO-1449	Document Number (Case)	Application Number	
INFORMATION DISCLOSURE CITATION IN AN APPLICATION		TSMC - 00-004	09/604,067
(Use several sheets if necessary)		Applicant	Ming-Dou Ker et al.
		Filing Date	06/26/00
		Drawn At U.S.	

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Amerasekera et al., "Substrate Triggering and Salicide Effects on ESD Performance and Protection Circuit Design in Deep Submicron CMOS Processes", IEDM Tech Digest, 1995, pp. 547-550.

Anderson et al., "ESD Protection for Mixed-Voltage I/O Using NMOS Transistors Stacked in a Cascode Configuration", Proc. of EOS/ESD

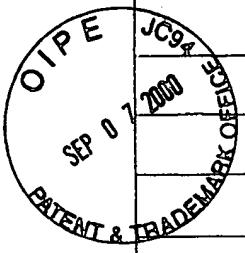
Symp., pp. 54-62, 1998. DATE CONSIDERED,

1/8/03

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Form PTO-1449	Document Number (Open)	Application Number
INFORMATION DISCLOSURE CITATION IN AN APPLICATION		TSMC-00-004 09/604,067
(Use several sheets if necessary)		Applicant Ming - Dou Ker et al.
Filing Date 06/26/00		Group Art Unit

U. S. PATENT DOCUMENTS



FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS (*Including Author, Title, Date, Portion or Pages, Etc.*)

Chen et al., "Design Methodology and Optimization of Gate-Driven NMOS ESD Protection Circuits in Submicron CMOS Processes", IEEE Trans. on Electron Devices, Vol. 45, No. 12, pp. 2448 - 2456, Dec. 1998.

EXAMINER	DATE CONSIDERED
<i>Sabrina Polking</i>	1/8/03

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